Read-In Integrated Circuits for Large-format Multi-chip Emitter Arrays

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Abstract: *Conventional read-in integrated circuit (RIIC) designs use a layout approach where a single emitter pixel is duplicated and formed into an array. On the periphery of the emitter pixel array are the addressing circuits and wire bond pads are placed. This layout approach cannot be used for multi-chip RIIC arrays with Through Substrate Vias (TSVs) because there is no room for decoder and I/O circuits on the periphery of the chip. Also the diameter of the TSV is much larger than the pixel pitch (e.g. TSV diameter is typically 100-microns while emitter pixel pitch is 48-microns). Our paper describes a novel RIIC design to overcome this using a novel layout approach that distributes address decoding circuits and TSVs throughout the driver array. The paper also discusses a novel abuttment method for creating multi-chip arrays. A prototype RIIC chip has been designed and fabricated using ONSEMI C5N process to verify our approach.*

Keywords: Large scale arrays; Tiling; Mosaic; Abutment; IR Scene Projection; Infra-red LED arrays

Introduction

A RIIC is a CMOS circuit array that is organized as a two dimensional array of pixels where each pixel integrates a driver and an optical or an infrared emitter. Various device technologies for light emission in RIICs including MEMS, thermal resistors, and LEDs. Typically, the optical emitters are mated with the CMOS RIIC using flip-chip bonding or post-foundry growth processes. The finished part is called a hybrid and the hybrid is packaged in a standard IC package for integration into an image projection system.

Recently, LED emitter devices have shown promise as a new high-power and a high-density light emission technology for use with RIICs. In particular, a 68 by 68 LED-based RIIC with 120 micron pitch [1] and 512 by 512 RIIC with 48 micron pitch [2] have been demonstrated. The 120 and 48 micron pixel designs have identical individual pixel circuits that have a complete LED driver, address selection and testability circuit. The finished 512 by 512 SLEDs hybrid is depicted in figure 1.

Infra-red image sensor development to larger format arrays has significantly outpaced infra-red scene projectors (IRSP). As such there is a need for large format IRSPs in order to properly test large format infra-red image sensors.

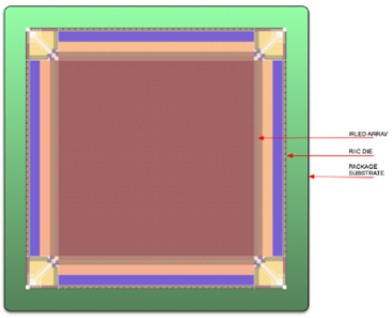

Figure 1. 512 x 512 48 micron pitch SLEDs hybrid

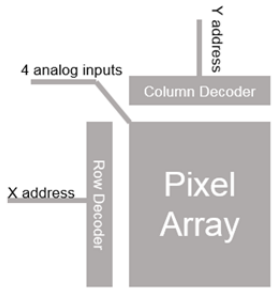

Figure 2. Single RIIC architecture

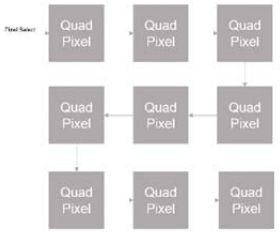

Figure 3. Edge-less RIIC architecture

Manufacturing single-chip RIICs beyond 1k by 1k in size is uneconomical due to yield considerations, and the limitations on scaling down the pixel size. For example, to manufacture a 2K by 2K RIIC with a 48 micron pixel pitch, the chip size is 14cm x 14 cm. At this chip size, only one RIIC chip can fit on a single 8" silicon wafer and the chip yield becomes nearly zero. The resulting cost to fabricate large monolithic arrays would be approximately one million dollars. Scaling down the pixel size would also yield a higher resolution projector. However, pixel size cannot be easily scaled down due to the scaling limits associated with light emission devices. As well as the high-voltage and high-current drive requirements of light emission devices: 10 - 20mA at 5 - 10V.

To overcome these challenges novel approaches that package multiple RIIC chips with TSV technology for improved IO and power delivery are being researched. A test chip with a scaled down version of the technology described in this paper has been fabricated.

For comparison a traditional single chip RIIC architecture is depicted in figure 2. While, in figure 3 an edge-less version of a RIIC with distributed addressing logic is shown.

Current RIIC Design

The current RIIC design has a unit cell of a single emitter pixel. This pixel includes circuitry for creating a voltage controlled current source, x and y coordinate addressing, and testing. It is depicted in figure 4. This pixel is duplicated to make a grid of pixels.

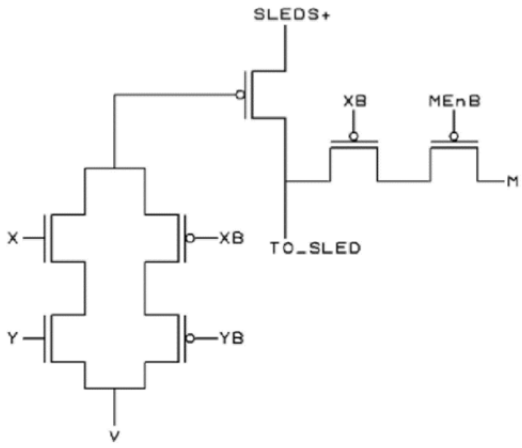

Figure 4. 48 micron pixel circuit

The layout for this RIIC design follows the circuit schematic fairly closely. Each pixel in the layout is the same unit cell repeated. The layout for a 4x4 48 micron layout is shown in figure 5.

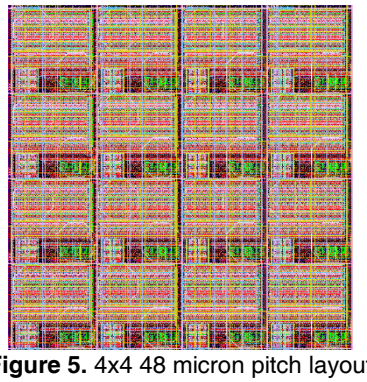

Figure 5. 4x4 48 micron pitch layout

On the periphery of the driver array wire-bond pads, and address decoding circuits are placed. In this RIIC design there is an abundance of space on the periphery of the device. This layout approach does not work for a multi-RIIC array architecture because any array larger than 2 by 2 will require a RIIC to be in the inner portion of the array and will not have room on the periphery for I/O circuits. To overcome this an edge-less RIIC was designed.

Edge-less RIIC Design

The edge-less RIIC design distributes address decoding, and power connections throughout the driver array. This removes the necessity of having these circuits on the periphery of the driver array. Through-silicon vias (TSV) are used to distribute input and output signals, and power throughout the driver array. This presents several design challenges because of the size of TSVs, and the low density with which TSVs can be placed in a design.

TSVs cause design challenges due to their large size, 100 microns. No active CMOS circuits may be placed on top of the TSV in this 100 micron zone. The TSV is much larger than the pixel pitch which makes it impossible to include a TSV in every pixel circuit. Pixels must share TSV resources as a result.

The low density with which TSVs can be placed in a design is caused by the large spacing rules, 271 microns, for the distance between two TSVs. This limits the total number of I/O signals and power that can be used on the RIIC. As a result of the low amount of inputs available and distributed addressing required it is more practical to use a scan chain style addressing system. The minimal amount of signals required to operate a RIIC with a scan chain architecture is 32. These inputs include 4 analog inputs for driving four SLEDs from 0V to VDD, addressing signals, shift register inputs and outputs, and circuit control voltages needed by the pixel circuit.

Hierarchical Organization: To enable sharing of resources in the RIIC several hierarchical structures were created: an edge-less pixel, a quad pixel, a RIIC side super pixel, and a sub-tile. The structures are listed in increasing size, but have different functions. These structures help create unit cells that can be repeated to make full-size RIICs of arbitrarily large size, while conserving layout space and sharing resources.

An edge-less pixel is very similar to the 48 micron pixel circuit found in the 512 by 512 RIIC. The change to a scan chain architecture only required the addition of analog memory between the two pass transistors. The analog memory is required because the second pass transistor activated by the “DISP” signal is now a global signal instead of a column select signal. The first pass transistor is selected by the “load” signal, which is no longer a row select signal.

A quad pixel is a grouping of four pixels together that share a flip-flop for storing the load command that activates the

first pass transistor. This saves layout space by sharing the flip-flop between the pixels and allows the four pixels to be written to simultaneously through the four analog input lines.

In order to create a unit cell that can be repeated a RIIC side super pixel was created. The function of the RIIC side super pixel is to share a TSV resource efficiently amongst pixels. In the test chip 32 pixels share one TSV. The RIIC side super pixel is shown in figure 6. The RIIC side super pixels are grouped together into a sub tile array.

The sub tile array is the smallest unit cell that can be fabricated as a complete chip. In the case of the test chip it is 1024 pixels and 32 TSVs arranged as a 16x64 pixel array. Multiple sub tiles can be attached together to create larger RIIC chips. For example, to make a 512x512 RIIC an array of 32 x 16 sub tiles are attached together. A sub tile array is shown in figure 7.

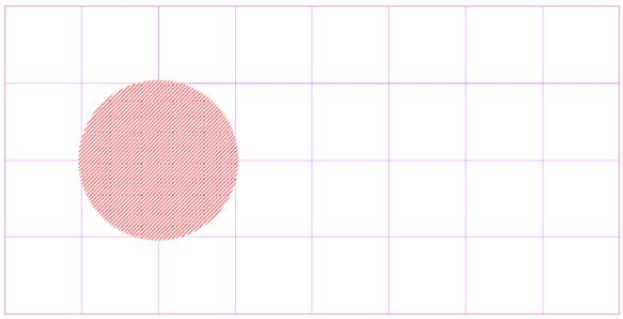

Figure 6. A RIIC-side super pixel. Each square contains an emitter and the red circle represents a TSV

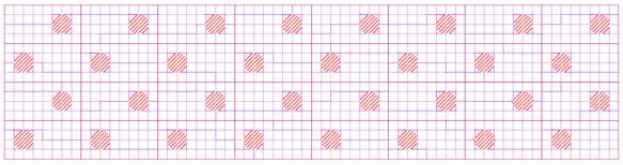

Figure 7. Sub tile layout

Scan Chain Addressing Operation: Scan chain addressing works by having serially connected nodes that pass the load signal down the "chain" until all nodes have received a new load signal. The load signal selects a specific quad pixel by setting the load bit high on the pass transistors in all four of the pixels in that quad pixel.

Once the first pass transistor is open it is then possible to store an analog value on the analog memory between the two pairs of pass transistors. This choice in addressing was chosen because any number of quad pixels can be in the chain and any number of RIICs can be connected together in an array. This is contrasted with a traditional x and y addressing grid where the more pixels there are in a projector the more address bits are required. X and y addressing is not a sustainable and easily expanded addressing architecture nor will it work well with abutted RIICs.

Abutment Method

Abutting RIICs into an array is challenging because of the precise positioning required to achieve a uniform image. This problem is a new design challenge because it is not seen in image sensor design. In figure 8 a typical pre-processed astronomical image is shown. The large spacing between the tiled image sensors is very apparent. However, the gaps in the image can be corrected during a post-processing step by taking the image from multiple angles and interpolating the data.

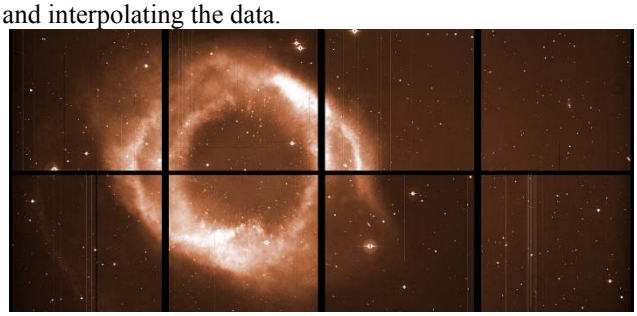

Figure 8. Helix nebula imaged with the Wide Field Imager at the La Silla Facility (photo credit: European Southern Observatory)

To create a uniform image with an abutted SLEDs based projector a spacing of 10 microns between the hybrids must be maintained. With a 10 micron spacing the lambertian distribution of light emission from the SLEDs [1] will hide the gap in the projected image.

A 10 micron spacing is challenging because of the large aspect ratio of the hybrids. A 10 micron spacing and tiling has been demonstrated by Indiana Integrated Circuits [3]. However, due to our novel architecture chip level interconnections are not necessary and a less expensive and less process intensive method is being developed.

To successfully align the hybrids with a 10 micron gap the edges of the hybrid must be cut precisely. Precise cutting will have to eliminate any protrusions from the edges of the hybrids that exceed 10 microns and would impede abutment of the hybrids. The proposed solution is to work in conjunction with Teledyne Technologies Inc. and develop an etching process that will successfully etch through the materials in the hybrid package.

The proposed solution for alignment of the hybrids is to print alignment marks on a piece of glass coated with a weak adhesive and use a lithography machine to place the hybrids on the glass. Then the aligned hybrids will be flipped onto a substrate and attached there. This method is depicted in figure 9.

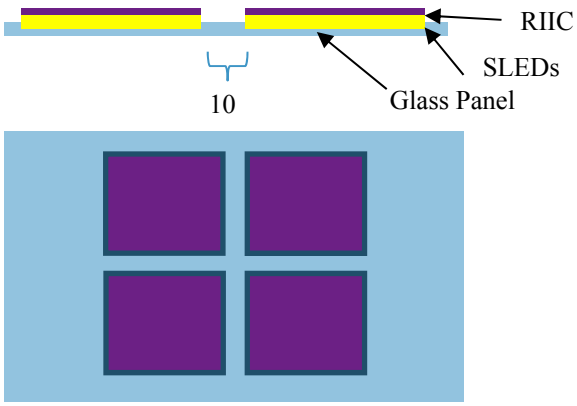

Figure 9. Aligned hybrids on a glass panel

Conclusion

A novel RIIC architecture has been designed and fabricated in a test chip to address the need for larger format scene projectors in the infra-red scene projection community. This new architecture comes with operational challenges that must be explored. One of these challenges that first comes to mind with this architecture is frame rate.

Frame rate is often a cited requirement for projectors and a serial connection has the limitation of trading speed for extensibility. However, this is an acceptable trade-off because of the quad pixel design and the speed with which modern digital logic can operate. Every sub-tile has four independent analog inputs. These analog inputs can be shorted together or left independent when stitching together sub-tiles to make a full scale RIIC of any frame rate desired.

For the 100Hz system control electronics there are four analog inputs writing in parallel and digital logic that can operate at approximately 100MHz. With this hardware and configuration it has been observed that a 1 KHz frame rate for a 512 x 512 RIIC can be achieved.

The test chip is currently being evaluated for complete functionality. Once the circuit architecture has been vetted the proposed alignment solution will be investigated more completely.

Acknowledgements

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(b) "Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Air Force Research Laboratory (AFRL) or the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program and/or the US Army Program Executive Office for Simulation, Training and Instrumentation (PEO STRI)."

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